Claims

1. Test switching circuit for a high speed data interface (1) of an integrated circuit comprising switching transistors (T1 - T6) which switch in a test mode a termination resistor output stage (15) of a data transmission signal path (17) to a termination resistor input stage (18) of a data reception signal path (25) to form an internal feedback test loop within said integrated circuit.

2. The test switching circuit according to claim 1 wherein the test switching circuit (26) is connected to a configuration register (29)

3. The test switching circuit according to claim 1 wherein the termination resistor output stage (15) is programmable.

4. The test switching circuit according to claim 1 wherein the termination resistor input stage (18) is programmable.

5. The test switching circuit according to claim 1 wherein the controllable test switching circuit (26) comprises:
a first transistor (T1) connected to said termination resistor output stage (15) of the data transmission signal path (17);
a second transistor (T2) connected between said first transistor (T1) and a reference potential node (GND);
a third transistor (T3) connected between said reference potential node (GND) and a sixth transistor (T6);
a fourth transistor (T4) connected between said first transistor (T1) and a test node (35);

a fifth transistor (T5) connected between said test node (35) and said sixth transistor (T6);
wherein the sixth transistor (T6) is connected to said termination resistor input stage (18) of the data reception signal path (25).

6. The test switching circuit according to claim 5 wherein the transistors (T1 - T6) are formed by MOSFETs.

7. The test switching circuit according to claim 6 wherein the gate terminals of the transistors (T1 - T6) are controlled by control bits (C1 - C6) stored in said configuration register (29).

8. The test switching circuit according to claim 5 wherein in a normal operation mode of said integrated circuit
the first transistor (T1) is switched off,
the second transistor (T2) is switched on,
the third transistor (T3) is switched on,
the fourth transistor (T4) is switched off,
the fifth transistor (T5) is switched off and
the sixth transistor (T6) is switched off.

9. The test switching circuit according to claim 5 wherein in a feedback test mode of said integrated circuit
the first transistor (T1) is switched on,
the second transistor (T2) is switched off,
the third transistor (T3) is switched off,
the fourth transistor (T4) is switched on,
the fifth transistor (T5) is switched on and
the sixth transistor (T6) is switched on.

10. The test switching circuit according to claim 5 wherein in a receiver test mode of said integrated

circuit
the first transistor (T1) is switched off,
the second transistor (T2) is switched off,
the third transistor (T3) is switched off,
the fourth transistor (T4) is switched off,
the fifth transistor (T5) is switched on and
the sixth transistor (T6) is switched on.

11. The test switching circuit according to claim 5 wherein in a transmitter test mode of said integrated circuit
the first transistor (T1) is switched on,
the second transistor (T2) is switched off,
the third transistor (T3) is switched off,
the fourth transistor (T4) is switched on,
the fifth transistor (T5) is switched off and
the sixth transistor (T6) is switched off.

12. The test switching circuit according to claim 5 wherein the controllable test switching circuit (26) is fully differential.

13. A high speed data interface (1) within an integrated circuit (IC) comprising:

(a) a transmitting signal path (17) for transmitting data via a data transmission line which is connected to a termination resistor output stage (15) of said data transmission signal path (17), wherein the termination resistor output stage (15) is provided for adapting the output impedance of said data transmission signal path (17) to a load connected to said transmission data line;

(b) a reception data signal path (25) for receiving data via a data reception line, which is

connected to a termination resistor input stage (18) of said data reception signal path (25), wherein the termination resistor input stage (18) is provided for adapting the input impedance of said data reception signal path (25) to a load connected to said reception data line; and

(c) a controllable test switching circuit (26) comprising switching transistors (T1 - T6) for switching in a test mode the termination resistor output stage (15) to the termination resistor input stage (18) to form an internal feedback test loop within said integrated circuit.

14. Integrated circuit having several high speed data interfaces (1), wherein each high speed data interface comprises:

(a) a transmitting signal path (17) for transmitting data via a data transmission line which is connected to a termination resistor output stage (15) of said data transmission signal path (17), wherein the termination resistor output stage (15) is provided for adapting the output impedance of said data transmission signal path (17) to a load connected to said transmission data line;

(b) a reception data signal path (25) for receiving data via a data reception line, which is connected to a termination resistor input stage (18) of said data reception signal path (25), wherein the termination resistor input stage (18) is provided for adapting the input impedance of said data reception signal path

(25) to a load connected to said reception data line; and

(c) a controllable test switching circuit (26) comprising switching transistors (T1 - T6) for switching in a test mode the termination resistor output stage (15) to the termination resistor input stage (18) to form an internal feedback test loop within said integrated circuit.